EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	718	716/3.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/10 16:30
L2	46	716/3.ccls. and (verilog or vhdl or hdl) near5 ("c++" or "c" or "cpp" or "c plus plus")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/10 16:31
S1	2457632	(compil$5 or convert$3 or conversion or translat$3 or transform$5 or (cross near3 compil$5) or reverse) and (verilog and "c++" or "c" or "cpp" or "c plus plus")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/09 17:58
S2	618	717/136.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/09 17:57
S3	189	717/137.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/09 17:57
S4	180	717/138.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/09 17:58
S5	286	717/139.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/09 17:58
S6	1495	(compil$5 or convert$3 or conversion or translat$3 or transform$5 or (cross near3 compil$5) or reverse) and (verilog and "c++" or "c" or "cpp" or "c plus plus") and 717/13?.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/09 17:58
S7	0	(compil$5 or convert$3 or conversion or translat$3 or transform$5 or (cross near3 compil$5) or reverse) and (verilog and "c++" or "c" or "cpp" or "c plus plus") and 717/13?.ccls. and "verilog to" near2 ("c++" or "cpp" or "c plus plus")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/09 18:00

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S8	4	(compil$5 or convert$3 or conversion or translat$3 or transform$5 or (cross near3 compil$5) or reverse) and (verilog and "c++" or "c" or "cpp" or "c plus plus") and 717/13?.ccls. and verilog near3 ("c++" or "cpp" or "c plus plus")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/09 18:09
S9	10	(compil$5 or convert$3 or conversion or translat$3 or transform$5 or (cross near3 compil$5) or reverse or map$4) and (verilog and "c++" or "c" or "cpp" or "c plus plus") and 717/13?. ccls. and (verilog or hdl or rtl or vhdl) near3 ("c++" or "cpp" or "c plus plus")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/09 18:20
S10	6	S9 not S8	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/09 18:10
S11	406	(compil$5 or convert$3 or conversion or translat$3 or transform$5 or (cross near3 compil$5) or reverse or map$4) same (verilog or hdl or rtl or vhdl) same ("c++" or "cpp" or "c plus plus")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/09 18:21
S12	176	(compil$5 or convert$3 or conversion or translat$3 or transform$5 or (cross near3 compil$5) or reverse or map$4) near5 (verilog or hdl or rtl or vhdl) same ("c++" or "cpp" or "c plus plus")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/09 18:24
S13	65	(compil$5 or convert$3 or conversion or translat$3 or transform$5 or (cross near3 compil$5) or reverse or map$4) near5 (verilog or hdl or rtl or vhdl) near5 ("c++" or "cpp" or "c plus plus")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/09 18:23
S14	1	(compil$5 or convert$3 or conversion or translat$3 or transform$5 or (cross near3 compil$5) or reverse or map$4) near5 (verilog or hdl or rtl or vhdl) same ("c++" or "cpp" or "c plus plus") and ("vbscript" or "visual basic script")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/09 18:25
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S16	136	(compil$5 or convert$3 or conversion or translat$3 or transform$5 or (cross near3 compil$5) or reverse or map$4) near5 (verilog or hdl or rtl or vhdl) same ("c++" or "cpp" or "c plus plus") and ("task library" or library or driver or header or interface or api)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/09 18:27
S17	64	(compil$5 or convert$3 or conversion or translat$3 or transform$5 or (cross near3 compil$5) or reverse or map$4) near5 (verilog or hdl or rtl or vhdl) same ("c++" or "cpp" or "c plus plus") and ("task library" or library or driver or header or interface or api) and (verilog or hdl or rtl or vhdl) near5 ("# delay" or "ifdef" or "{" or "}" or (register near3 definition) or assignment or event or switch or "case statement" or concat or concatenation or "#define" or const or constant or (bit near3 access$3)) and (substitut$3 or translat$3 or remov$3 or convert$3 or insert$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/09 18:34
S18	6	("6097212" | "6188975" | "6415420" | "6507947").PN. OR ("6606734").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2007/03/09 18:53

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IET JNL IET Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IET CNF IET Conference Proceeding

IEEE STD IEEE Standard

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Greaves, D.J.;
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1 Hardware/software co-simulation in a VHDL-based test bench approach
Matthias Bauer, Wolfgang Ecker
June 1997 **Proceedings of the 34th annual conference on Design automation DAC '9**
Publisher: ACM Press
Full text available: pdf(88.32 KB) Additional Information: full citation, abstract, referenc citings, index terms

Novel test bench techniques are required to cope with afunctional test complexity whi predicted to grow muchmore strongly than design complexity. Our test benchapproacl attacks this complexity by using a stronghierarchical architecture, application domain independentsynchronization, reusable modules, and easy incrementalextendability bas table-driven techniques. In addition,the integration of VHDL/C co-simulation under tl controlof the test bench makes it possible to use the hardware ...

2 System level design research in an industrial setting (invited talks): IP reuse in the syste chip era
Warren Savage, John Chilton, Raul Camposano
September 2000 **Proceedings of the 13th international symposium on System synthe ISSS '00**
Publisher: IEEE Computer Society
Full text available: pdf(728.70

KB) Additional Information: full citation, abstract, referenc

Intellectual Property (IP) Reuse is one of the keys for System on a Chip (SoC) design productivity improvement. Although IP reuse has been explored both technically and business for many years, only recently systematic approaches based on EDA technolo starting to emerge in the marketplace. This paper gives an introduction to IP creation, conversion and the necessary infrastructure. We address the technical challenges and that a strict quality based design methodology is the co ...

3 Testing: On automatic generation of RTL validation test benches using circuit testing techniques

Indradeep Ghosh, Srivaths Ravi

April 2003 **Proceedings of the 13th ACM Great Lakes symposium on VLSI GLSVL**

Publisher: ACM Press

Full text available: pdf(145.00 KB) Additional Information: full citation, abstract, referenc index terms

In this paper, we examine how good validation test benches can be automatically gen starting from the RTL description of a circuit. We develop our methodology based on extensive experiments performed with several popular benchmarks as well as industri circuits.

Keywords: ATPG, OCCOM, RTL ATPG, RTL testing, branch coverage, code cover coverage metrics, design validation, fault coverage, generation, path coverage, small validation, test, test sets, testbench, testing, toggle coverage, universal test sets

4 A framework for object oriented hardware specification, verification, and synthesis

T. Kuhn, T. Oppold, M. Winterholer, W. Rosenstiel, Marc Edwards, Yaron Kashai

June 2001 **Proceedings of the 38th conference on Design automation DAC '01**

Publisher: ACM Press

Full text available: pdf(222.17 KB) Additional Information: full citation, abstract, referenc citings, index terms

We describe two things. First, we present a uniform framework for object oriented specification and verification of hardware. For this purpose the object oriented langua is introduced along with a powerful run-time environment that enables the designer to perform the verification task. Second, we present an object oriented synthesis that enl "e" and its dedicated run-time environment into a framework for specification, verific

and synthesis. The usab ...

Keywords: high-level synthesis, object oriented hardware modeling, verification

5 Special Session on Design Paradigms: SystemC: a modeling platform supporting multip design abstractions
Preeti Ranjan Panda
September 2001 **Proceedings of the 14th international symposium on Systems synth ISSS '01**
Publisher: ACM Press
Full text available: pdf(103.89 KB) Additional Information: full citation, abstract, referenc citings, index terms

SystemC is a C++ based modeling platform supporting design abstractions at the regi transfer, behavioral, and system levels. Consisting of a class library and a simulation l the language is an attempt at standardization of a C/C++ design methodology, and is supported by the Open SystemC Initiative (OSCI), a consortium of a wide range of sy houses, semiconductor companies, Intellectual property (IP) providers, embedded sofi developers, and design automation tool vendors. The adv ...

Keywords: C/C++ based design, SystemC, hardware description language, system le design

6 A system-level co-verification environment for ATM hardware design
G. Post, A. Müller, T. Grötker
February 1998 **Proceedings of the conference on Design, automation and test in Eur DATE '98**
Publisher: IEEE Computer Society
Full text available: pdf(69.33 KB) Publisher Site Additional Information: full citation, abstract, referenc citings, index terms

Common approaches to hardware implementation of networking components start at t VHDL level and are based on the creation of regression test benches to perform simul validation of functionality. The time needed to develop test benches has proven to be significant bottleneck with respect to time-to-market requirements. In this paper, we

describe the coupling of a telecommunication network simulator with a VHDL simula and a hardware test board. This co-verification approach enables the ...

Keywords: co-verification, test bench design and reuse, co-simulation, ATM hardwai design, system design methodology, interface modeling

7 Moving towards more effective validation: A comparison of three verification technique directed testing, pseudo-random testing and property checking
Mike G. Bartley, Darren Galpin, Tim Blackmore
June 2002 **Proceedings of the 39th conference on Design automation DAC '02**
Publisher: ACM Press
Full text available: pdf(212.50 KB) Additional Information: full citation, abstract, referenc citings, index terms

This paper describes the verification of two versions of a bridge between two on-chip The verification was performed just as the Infineon Technologies Design Centre in Bi was introducing pseudo-random testing (using Specman) and property checking (usin GateProp) into their verification flows and thus provides a good opportunity to compa these two techniques with the existing strategy of directed testing using VHDL bus functional models.

8 Automatic test bench generation for validation of RT-level descriptions: an industrial experience
F. Corno, M. Sonza Reorda, G. Squillero, A. Manzone, A. Pincetti
January 2000 **Proceedings of the conference on Design, automation and test in Euro DATE '00**
Publisher: ACM Press
Full text available: pdf(200.61 KB) Publisher Site Additional Information: full citation, references, citing index terms

9 Simulation-guided property checking based on a multi-valued AR-automata
J. Ruf, D. Hoffmann, T. Kropf, W. Rosenstiel
March 2001 **Proceedings of the conference on Design, automation and test in Europ**

DATE '01
Publisher: IEEE Press
Full text available: pdf(135.29 KB) Additional Information: full citation, references, citing index terms

10 Design Technology for Networked Reconfigurable FPGA Platforms
S. Guccione, D. Verkest, I. Bolsens
March 2002 **Proceedings of the conference on Design, automation and test in Europ DATE '02**
Publisher: IEEE Computer Society
Full text available: pdf(264.20 KB) Additional Information: full citation, abstract, citings

Future networked appliances should be able todownload new services or upgrades fro networkand execute them locally. This flexibility is typicallyachieved by processors tl download new softwareover the network, using JAVA technology. This paperdemons that FPGAs are a realistic implementationplatform for thin server or client application FPGAscan offer the same end-user experience as softwarebased systems, combined w more computationalpower and lower cost.

11 New topics in logic synthesis: Verilog HDL, powered by PLI: a suitable framework for describing and modeling asynchronous circuits at all levels of abstraction
Arash Saifhashemi, Hossein Pedram
June 2003 **Proceedings of the 40th conference on Design automation DAC '03**
Publisher: ACM Press
Full text available: pdf(218.74 KB) Additional Information: full citation, abstract, referenc index terms

In this paper, we show how to use Verilog HDL along with PLI (Programming Langu Interface) to model asynchronous circuits at the behavioral level by implementing CS (Communicating Sequential Processes) language constructs. Channels and communic actions are modeled in Verilog HDL as abstract actions.

Keywords: CHP, CSP, PLI, asynchronous circuits, channel, verilog

12 Behavioral synthesis methodology for HDL-based specification and validation

D. Knapp, T. Ly, D. MacMillen, R. Miller
January 1995 **Proceedings of the 32nd ACM/IEEE conference on Design automatio '95**
Publisher: ACM Press
Full text available: pdf(51.94 KB) Additional Information: full citation, references, citing index terms

13 IP Design and Reuse: Application of Software design patterns to DSP library design
Pontus Åström, Stefan Johansson, Peter Nilsson
September 2001 **Proceedings of the 14th international symposium on Systems synth ISSS '01**
Publisher: ACM Press
Full text available: pdf(144.85 KB) Additional Information: full citation, abstract, referenc citings, index terms

The design of a hardware data path library is one of the harder problems in design for Thanks to the appearance of hardware modeling libraries based on C++, it is possible apply advanced software techniques to design such a library. This paper shows how s design patterns can be applied to hardware design. Design patterns yield a twofold advantage: a faster design process, and a library that is more extensible and modular t equivalent HDL counterpart. From a VHDL-C++ design ...

14 A C-based synthesis system, Bach, and its application (invited talk)
Takashi Kambe, Akihisa Yamada, Koichi Nishida, Kazuhisa Okada, Mitsuhisa Ohnishi, Andrew Kay, Paul Boca, Vince Zammit, Toshio Nomura
January 2001 **Proceedings of the 2001 conference on Asia South Pacific design auto ASP-DAC '01**
Publisher: ACM Press
Full text available: pdf(69.87 KB) Additional Information: full citation, abstract, referenc citings, index terms

In system LSI design, a desirable system is one that allows the designer to describe, partition, and verify systems, and to generate circuits efficiently. In this paper, we des C-based system LSI design system called Bach which we have developed. Using the example of an MEPG-4 video codec design, we summarize its design flow, effects an current issues.

15 Verification of configurable processor cores
Marinés Puig-Medina, Gülbin Ezer, Pavlos Konas
June 2000 **Proceedings of the 37th conference on Design automation DAC '00**
Publisher: ACM Press
Full text available: pdf(79.05 KB) Additional Information: full citation, abstract, referenc citings

This paper presents a verification methodology for configurable processor cores. The simulation-based approach uses directed diagnostics and pseudo-random program gen both of which are tailored to specific processor instances. A configurable and extensit bench serves as the framework for the verification process and offers components nec for the complete SOC verification. Coverage analysis provides an evaluation of how v specific design has been exercised, of the br ...

Keywords: co-simulation, configurable processor cores, coverage analysis, design verification, system-on-chip, test generation

16 Functional test generation for behaviorally sequential models
F. Ferrandi, G. Ferrara, D. Sciuto, A. Fin, F. Fummi
March 2001 **Proceedings of the conference on Design, automation and test in Europ DATE '01**
Publisher: IEEE Press
Full text available: pdf(145.75 KB) Additional Information: full citation, references, citing index terms

17 Functional verification—real users, real problems, real opportunities (panel)
Jonah McLeod, Nozar Azarakhsh, Glen Ewing, Paul Gingras, Scott Reedstrom, Chris R
June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation D/**
Publisher: ACM Press
Full text available: pdf(21.27 KB) Additional Information: full citation, citings, index ter

18 Decomposition of timed decision tables and its use in presynthesis optimizations
Jian Li, Rajesh K. Gupta

November 1997 **Proceedings of the 1997 IEEE/ACM international conference on Computer-aided design ICCAD '97**

Publisher: IEEE Computer Society

Full text available: pdf(260.76 KB) Publisher Site

Additional Information: full citation, abstract, referenc citings, index terms

Presynthesis optimizations transform a behavioral HDL description into an optimized description that results in improved synthesis results. We introduce the decompositior timed decision tables (TDT), a tabular model of system behavior. The TDT decompos based on the kernel extraction algorithm. By experimenting using named benchmarks demonstrate how TDT decomposition can be used in presynthesis optimizations.

Keywords: TDT decomposition, behavioral HDL description, benchmarks, circuit sy decision tables, kernel extraction algorithm, optimized HDL description, presynthesis optimizations, system behavior model, timed decision table decomposition

19 A VHDL-based methodology for the design and verification of pipeline A/D converters

Eduardo Peralías, Antonio J. Acosta, Adoración Rueda, José L. Huertas

January 2000 **Proceedings of the conference on Design, automation and test in Euro DATE '00**

Publisher: ACM Press

Full text available: pdf(189.55 KB) Publisher Site

Additional Information: full citation, references, citing index terms

20 High Level and Architectural Synthesis: Object oriented hardware synthesis and verifica

T. Kuhn, T. Oppold, C. Schulz-Key, M. Winterholer, W. Rosenstiel, M. Edwards, Y. Ka

September 2001 **Proceedings of the 14th international symposium on Systems synth ISSS '01**

Publisher: ACM Press

Full text available: pdf(96.62 KB)

Additional Information: full citation, abstract, referenc citings, index terms

The synthesis of hardware from object oriented specifications is presented. Our appro utilizes the ***e*** language that has been proven to be highly efficient for the verification c hardware. The ***e*** language is similar to Java and provides additional constructs for specification and verification of hardware. We describe an automated design flow for synthesis of object oriented descriptions that tightly integrates simulation based verifi The usability of our a ...

Keywords: high-level synthesis, object oriented hardware modeling, verification

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EDACafe Weekly : SystemVerilog in the news (again) - October 13, 2003

David Greaves is a Professor in the Computer Science Laboratory at Cambridge ... I first heard of **Verilog** when I was at Silicon Graphics back in 1988. ...
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